

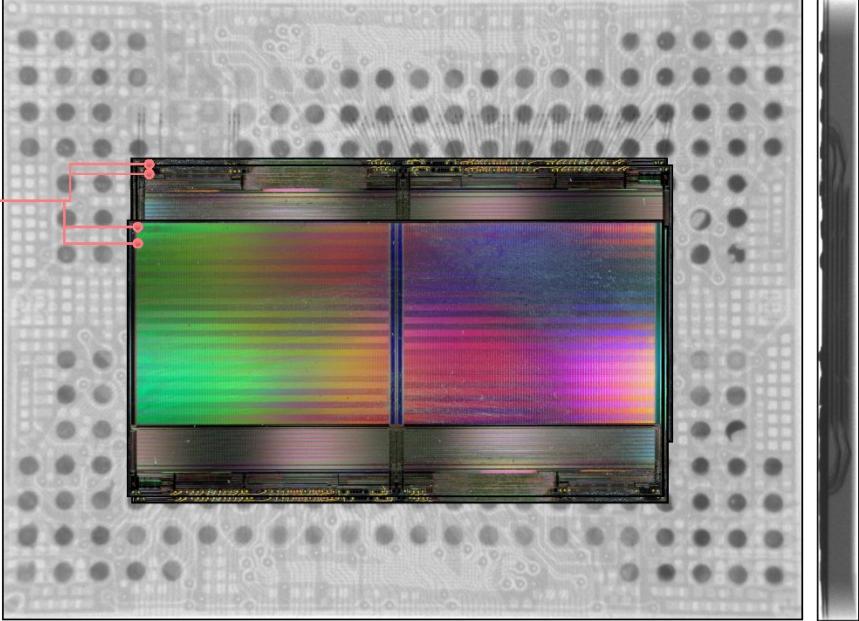
# EXHIBIT C

**U.S. Patent No. 6,724,241 (“241 Patent”)**

Dell/EMC products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the Dell/EMC XPS 15 2-in-1 9575 (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent. While the infringing structure and functionality of the Accused Products is illustrated below using the Dell/EMC XPS 15 2-in-1 9575 as an example, all Accused Products operate in substantially the same way for purposes of infringement.

**Claim 1**

Claim 1	Accused Products
1 [pre]. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.  For example, the Dell/EMC XPS 15 2-in-1 9575 includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.  <i>See, e.g.:</i>

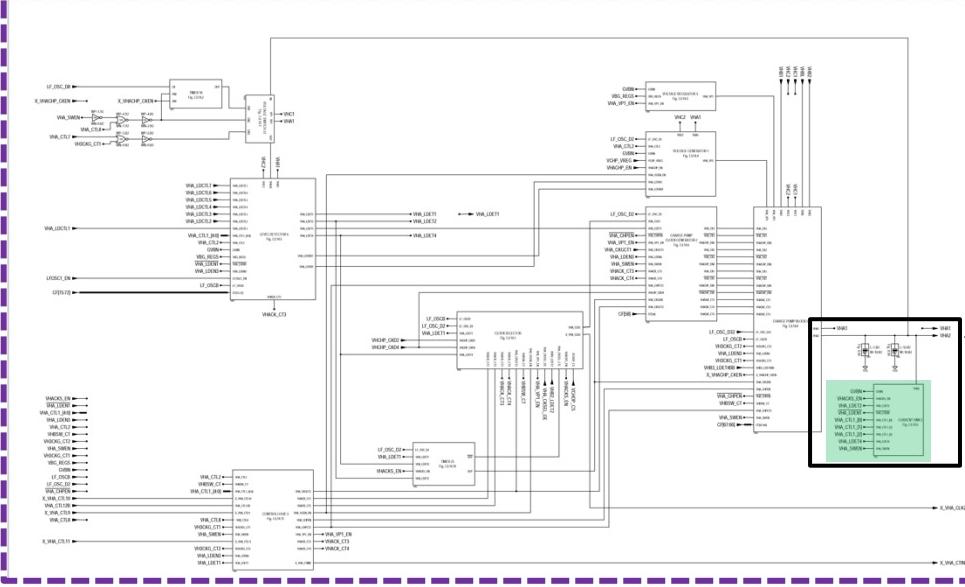
Claim 1	Accused Products
	<p>76 - Toshiba #TH58TFT0123BADE Multichip Memory - 128 GB 3D TLC NAND Flash (4-Die Pkg.) Pkg Size: 18.02 x 14.01 mm</p> <p>76.1 - Toshiba #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.15 x 6.28 mm</p> <p>Function: Memory: Non-Volatile</p>  <p>Source: TechInsights Deep Dive Teardown, Dell/EMC XPS 15 2-in-1 9575 ID306753-GDd</p>

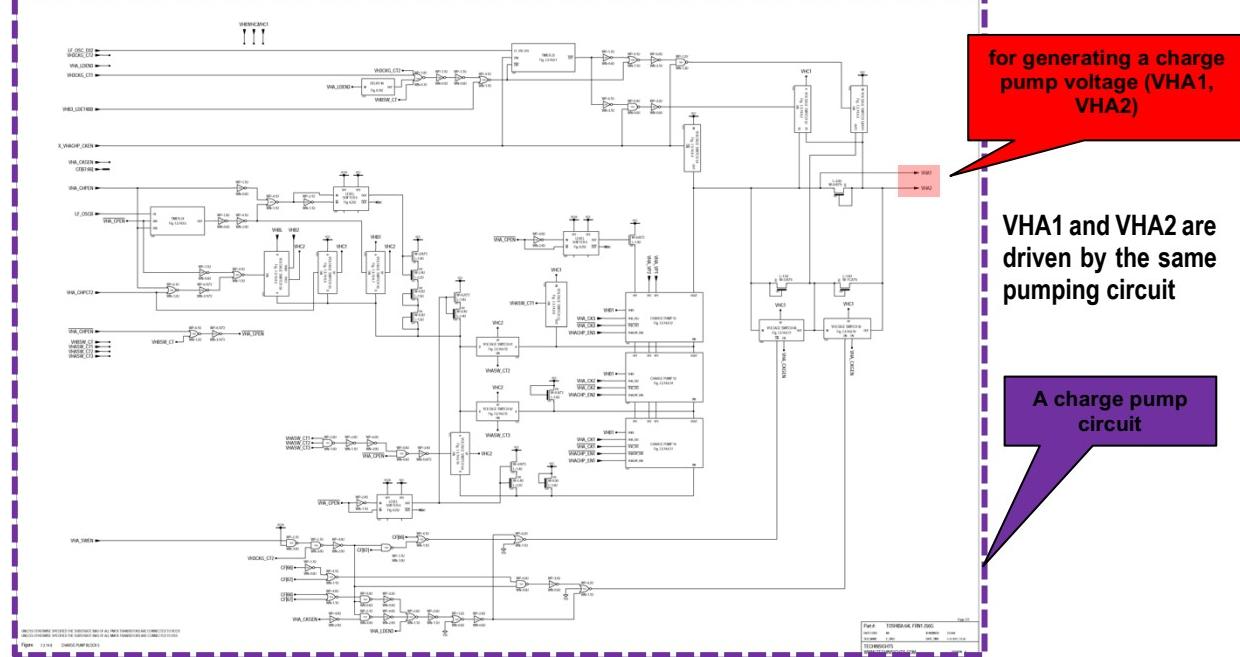
**Claim 1**

**Accused Products**

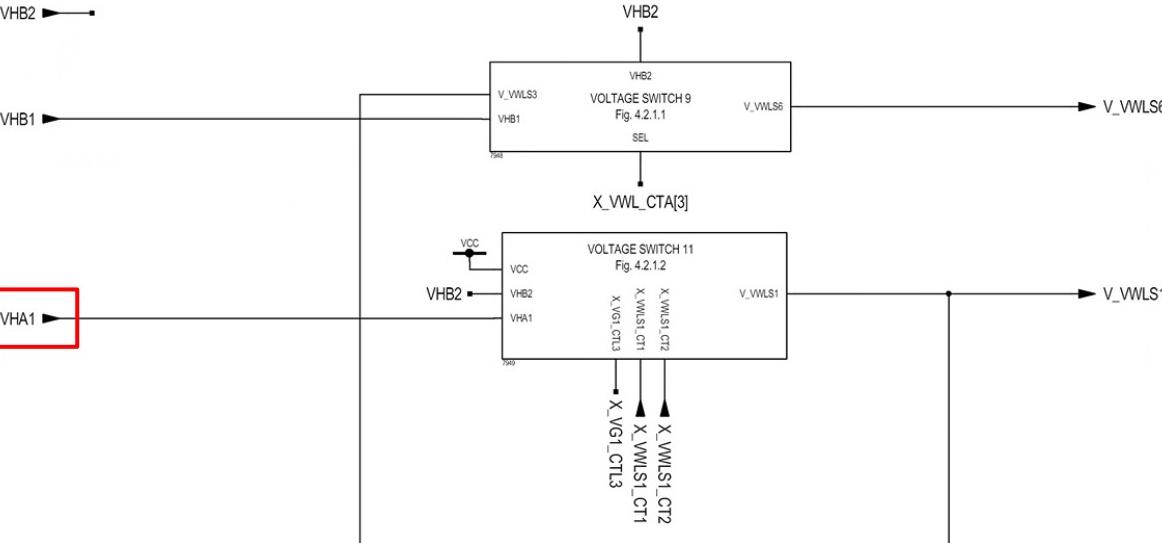
**VHA1**  
**VHA2**

**A charge pump circuit**

Claim 1	Accused Products
	 <p data-bbox="1664 736 1812 878" style="background-color: green; color: white; padding: 5px;">having minimal voltage ripples</p> <p data-bbox="635 926 1839 997">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3 Charge Pump System</p>

Claim 1	Accused Products
	 <p data-bbox="635 997 1839 1070">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Products
	<p style="color: red; font-weight: bold;">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>

Claim 1	Accused Products
	<p><b>Charge pump output voltage VHA1</b> is provided to high voltage switches to selectively drive wordline circuits.</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
1[a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit of the Dell/EMC XPS 15 2-in-1 9575, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHB1. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the</p>

Claim 1	Accused Products
	<p>output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

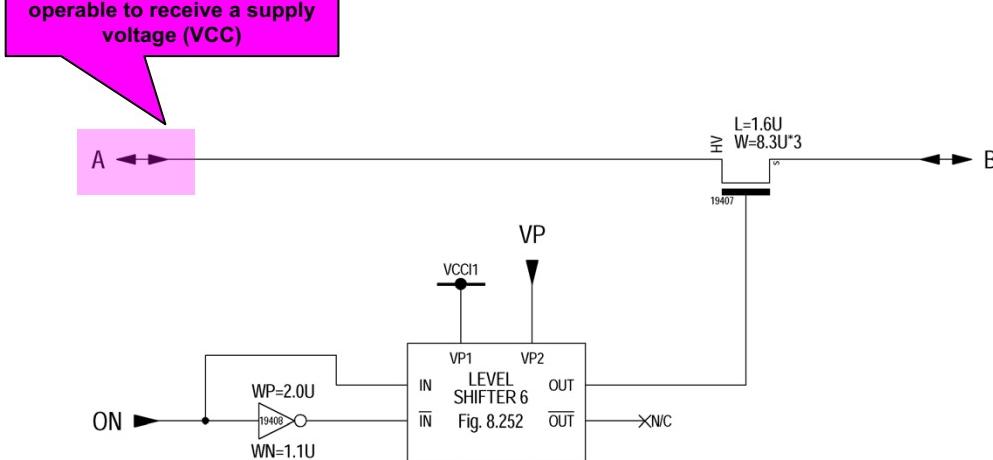
**Claim 1**

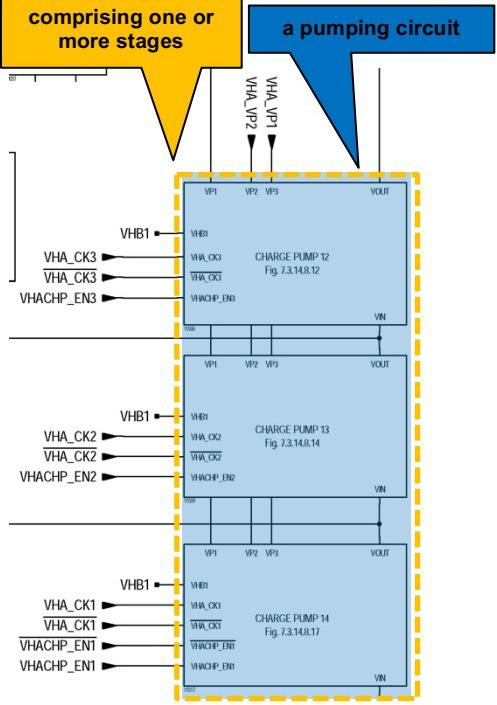
**Accused Products**

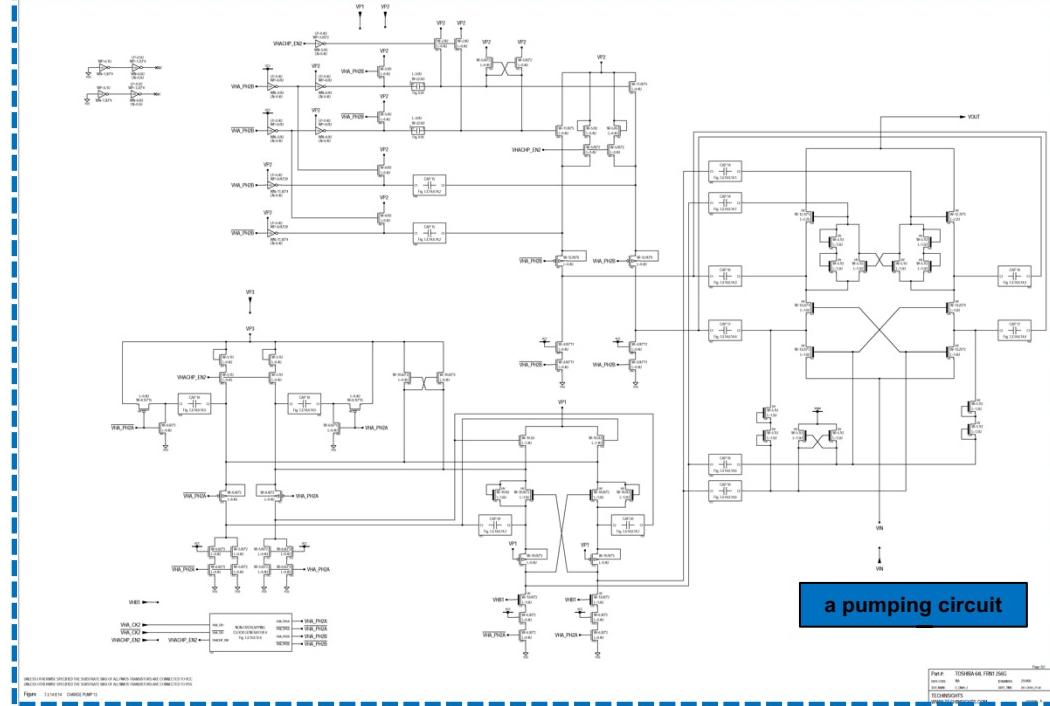
**operable to receive a supply voltage**

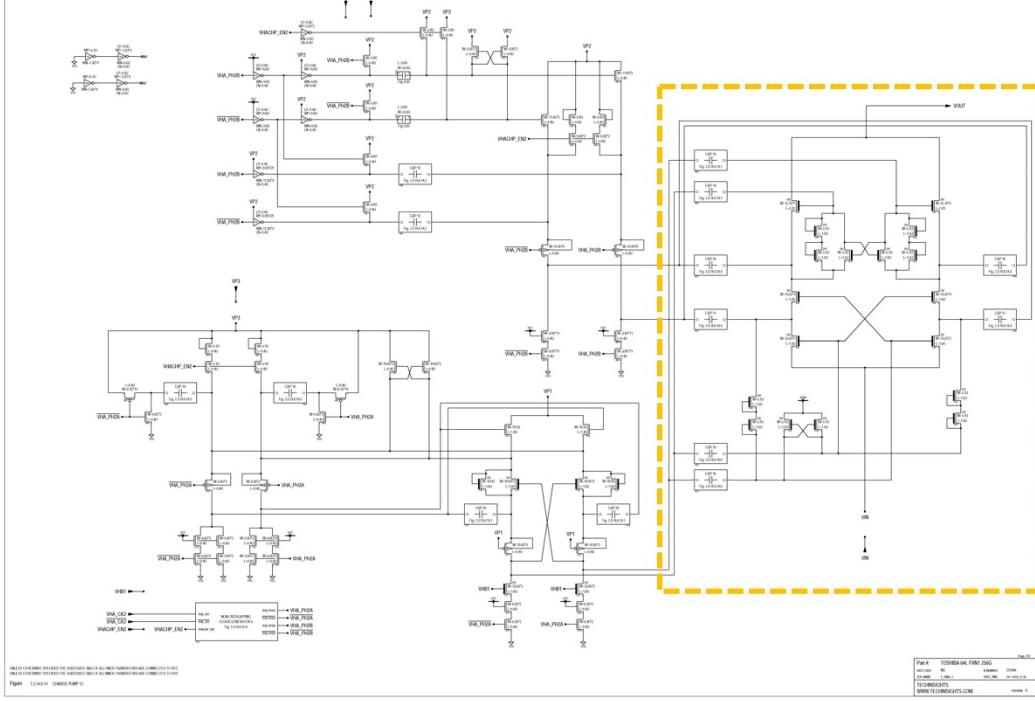
**a pumping circuit**

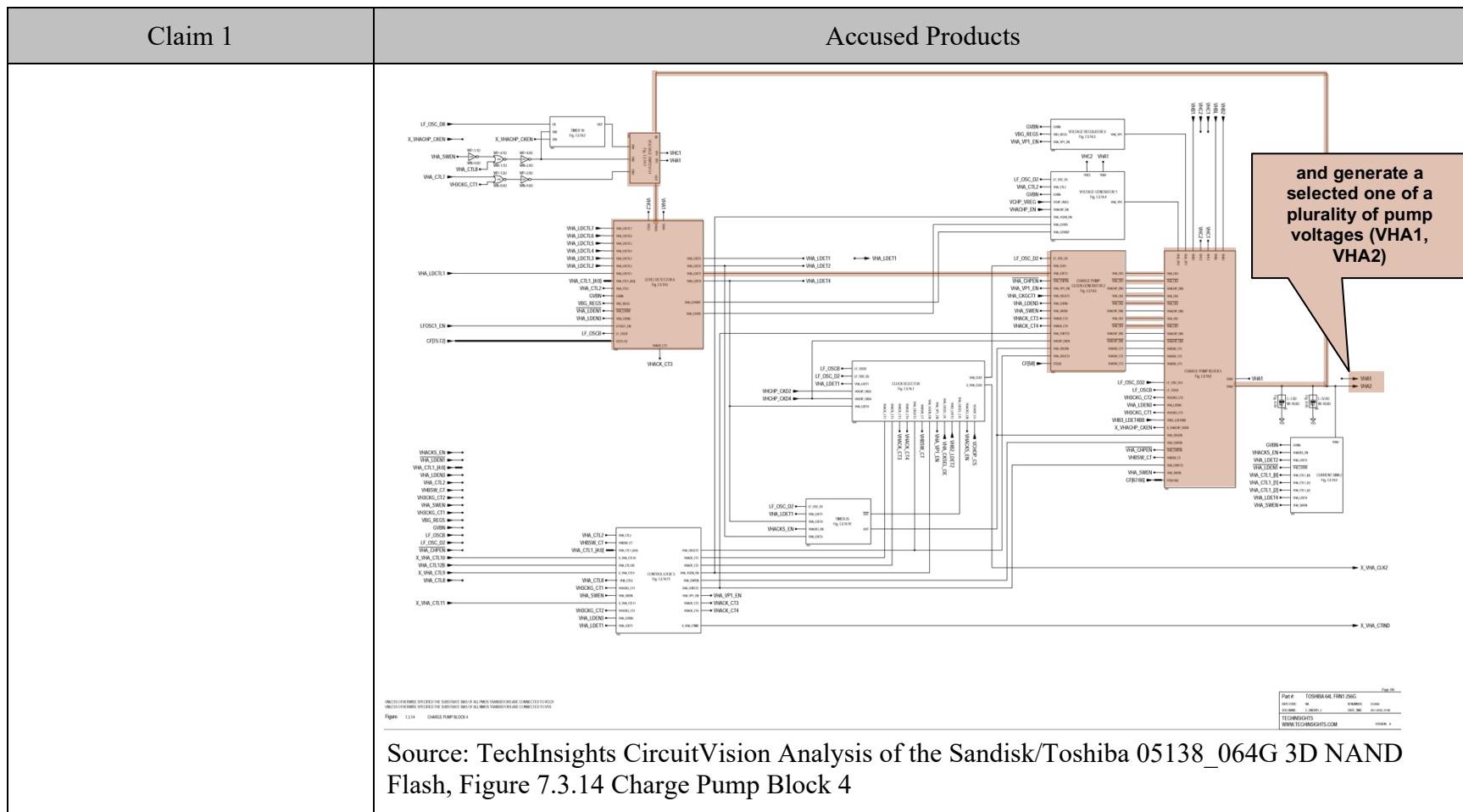
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138\_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

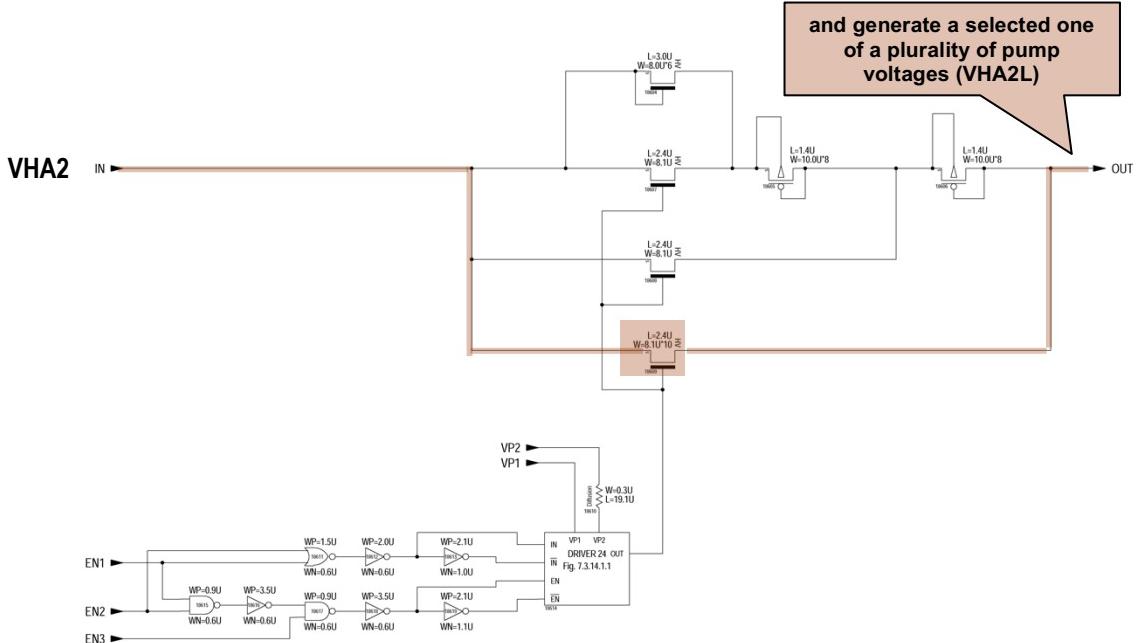
Claim 1	Accused Products
	<p>operable to receive a supply voltage (VCC)</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

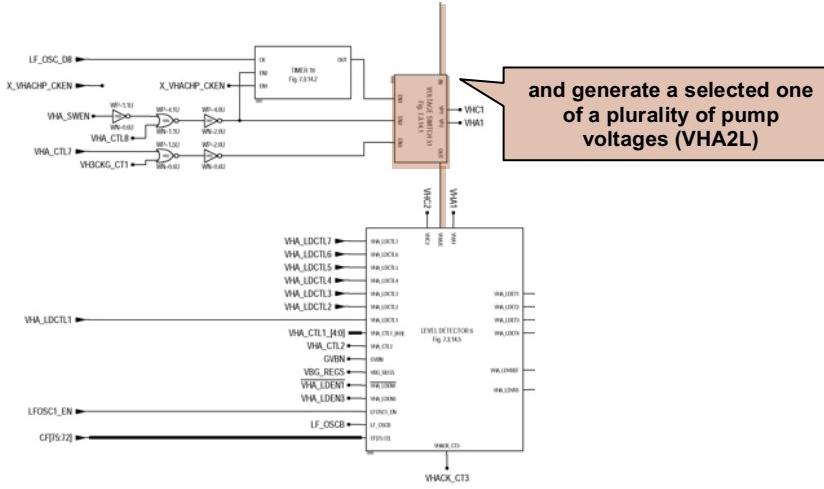
Claim 1	Accused Products
	 <p data-bbox="639 975 1136 1062">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Products
	 <p data-bbox="635 1041 1839 1111">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

Claim 1	Accused Products
	 <p data-bbox="635 943 1670 975">     Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13   </p>



Claim 1	Accused Products
	 <p data-bbox="650 905 1790 1070">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.1 Voltage Switch 51</p>

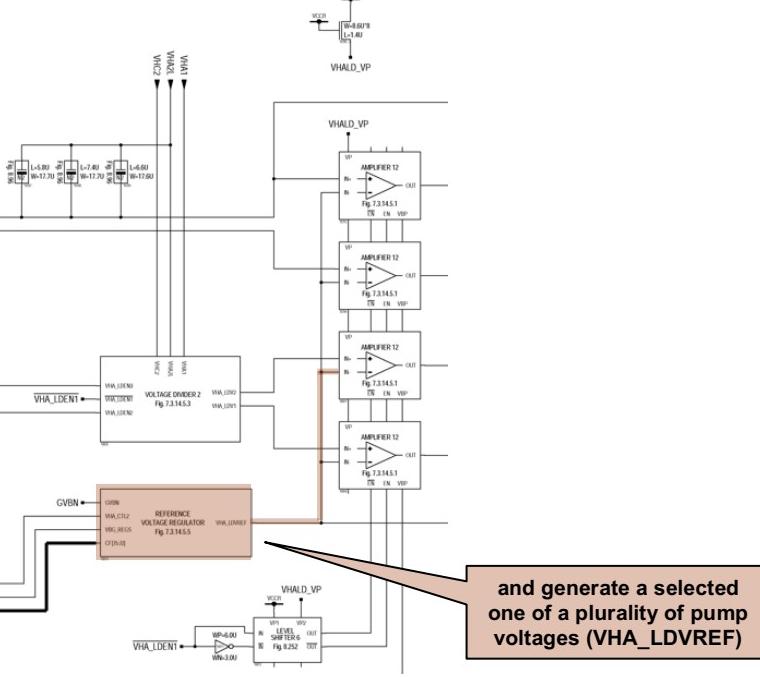
Claim 1	Accused Products
	 <p data-bbox="1184 404 1495 474"><b>and generate a selected one of a plurality of pump voltages (VHA2L)</b></p> <p data-bbox="639 837 1839 907">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

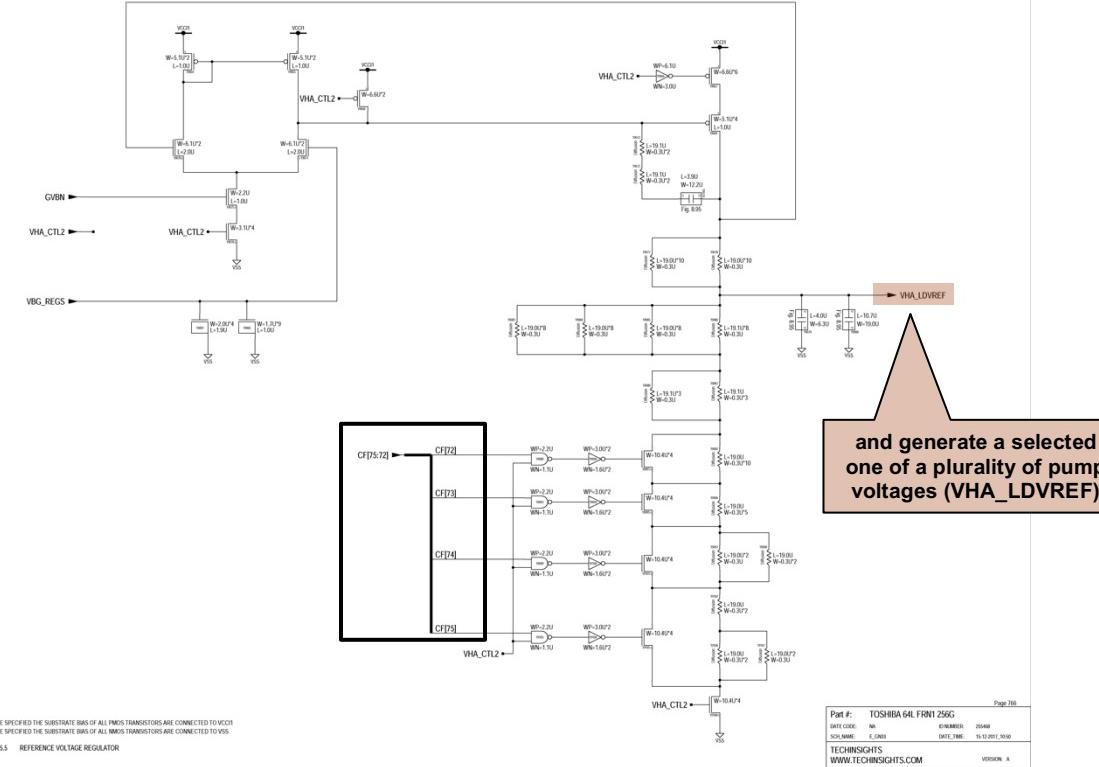
**Claim 1**

**Accused Products**

The diagram shows the circuitry for generating pump voltages. It includes two level detector blocks (LDEN1 and LDEN2), a resistor network (RES 5), and a voltage divider section. The output of the voltage divider is connected to three amplifiers (AMPLIFIER 12) which provide feedback to the voltage regulator. A callout box highlights the generation of a selected one of a plurality of pump voltages (VHA\_LDV2).

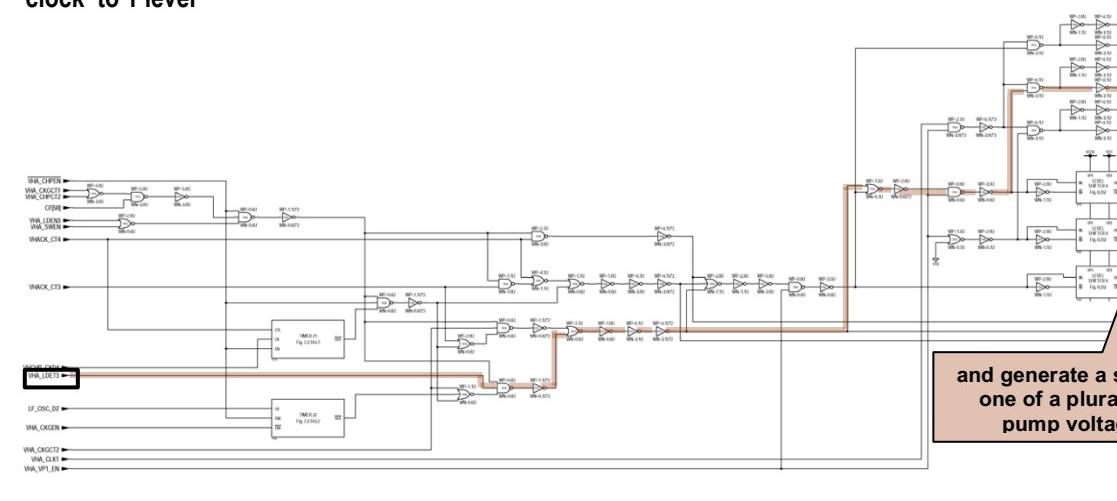
**and generate a selected one of a plurality of pump voltages (VHA\_LDV2)**

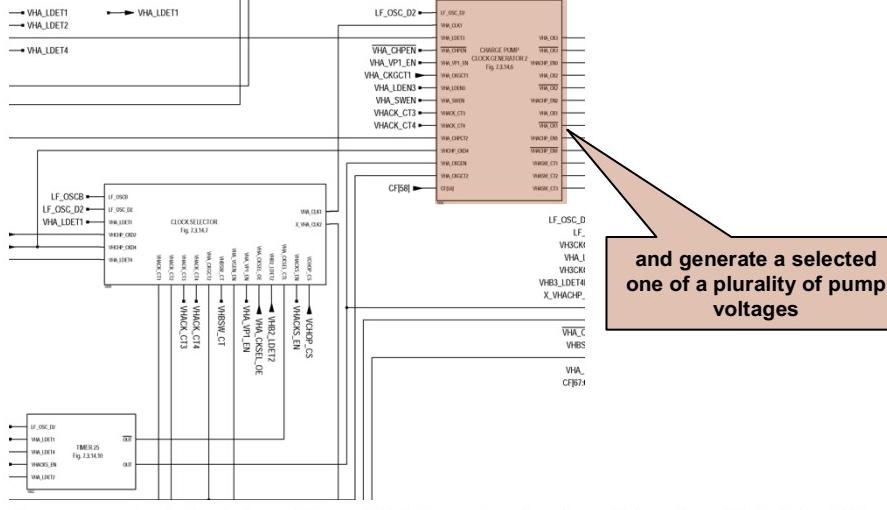
Claim 1	Accused Products
	 <p data-bbox="1151 856 1404 938"> <b>and generate a selected one of a plurality of pump voltages (VHA_LDVREF)</b> </p> <p data-bbox="623 995 1848 1077">     Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6   </p>

Claim 1	Accused Products
	 <p>UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL PMOS TRANSISTORS ARE CONNECTED TO VDD UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL NMOS TRANSISTORS ARE CONNECTED TO VSS</p> <p>Figure 7.3.14.5.5 REFERENCE VOLTAGE REGULATOR</p> <p>Part #: TOSHIBA 64L FRN1 256G DATE CODE: NA DRAWN BY: 20484 DESIGNED BY: 10/2017_AW TECHINSIGHTS WWW.TECHINSIGHTS.COM VERSION A</p> <p>Page 760</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator</p>

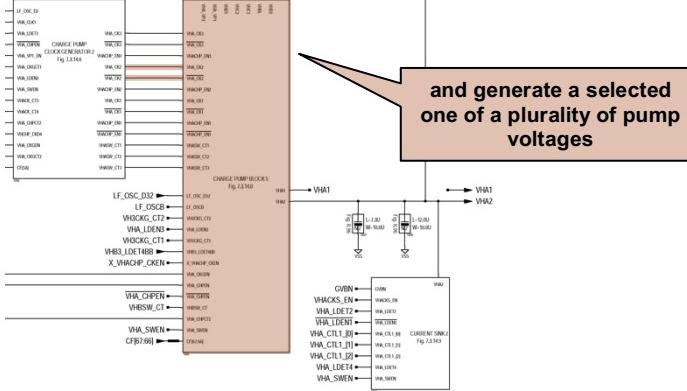


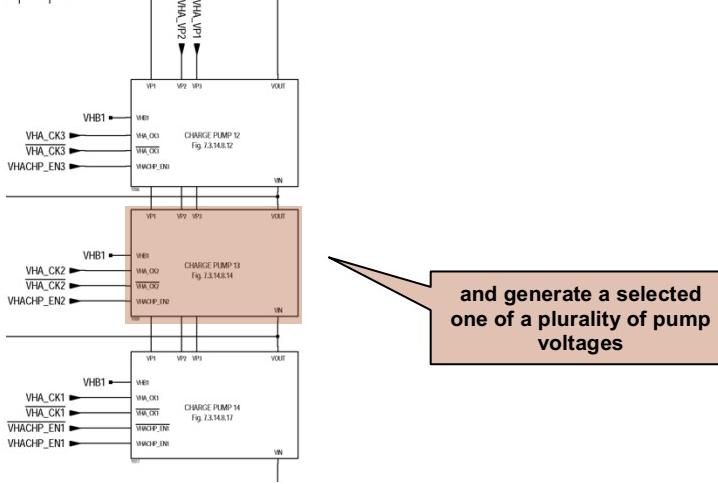


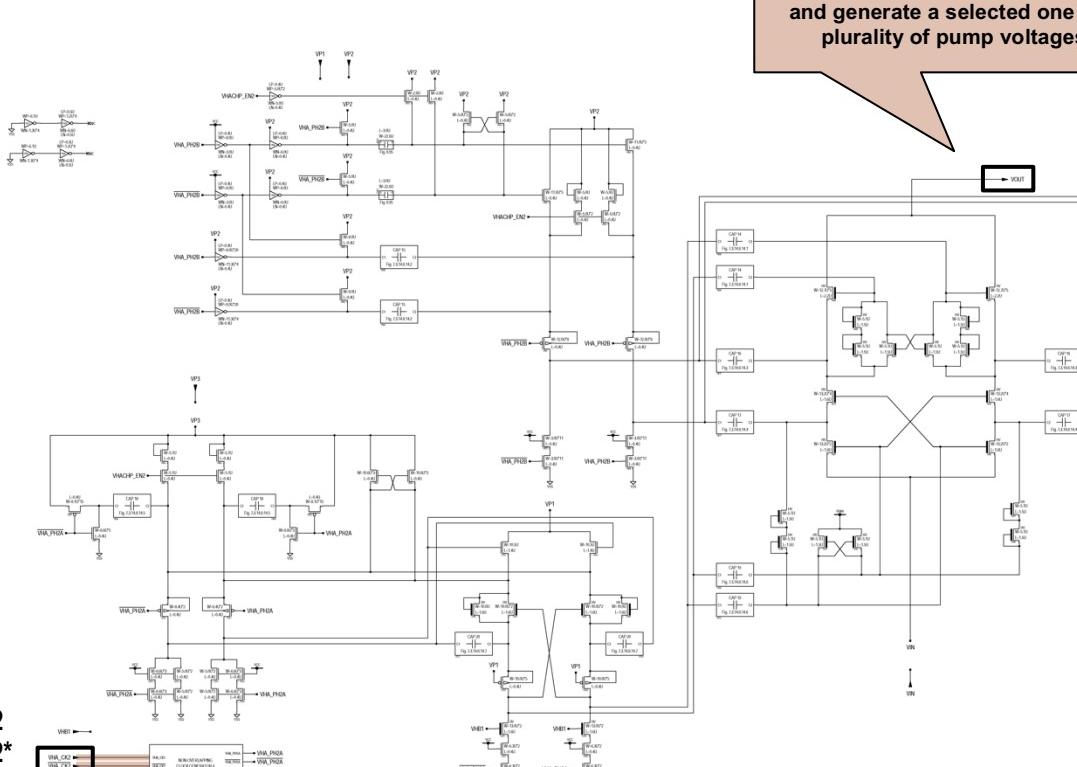
Claim 1	Accused Products
<p><b>VHA_LDET3 = 1</b>  <b>Disables VHA_CK2 pump clock to 1 level</b></p> 	<p><b>VHA_CK2 = 1</b>  <b>VHA_CK2* = 0</b></p> <p><b>and generate a selected one of a plurality of pump voltages</b></p>

Claim 1	Accused Products
	 <p data-bbox="629 780 1854 850">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

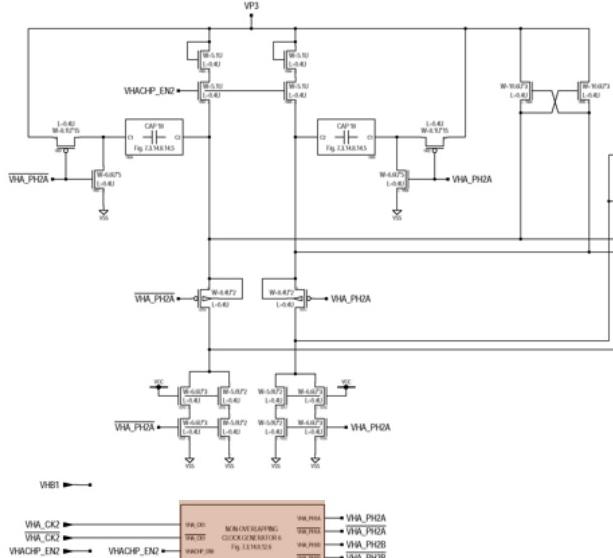


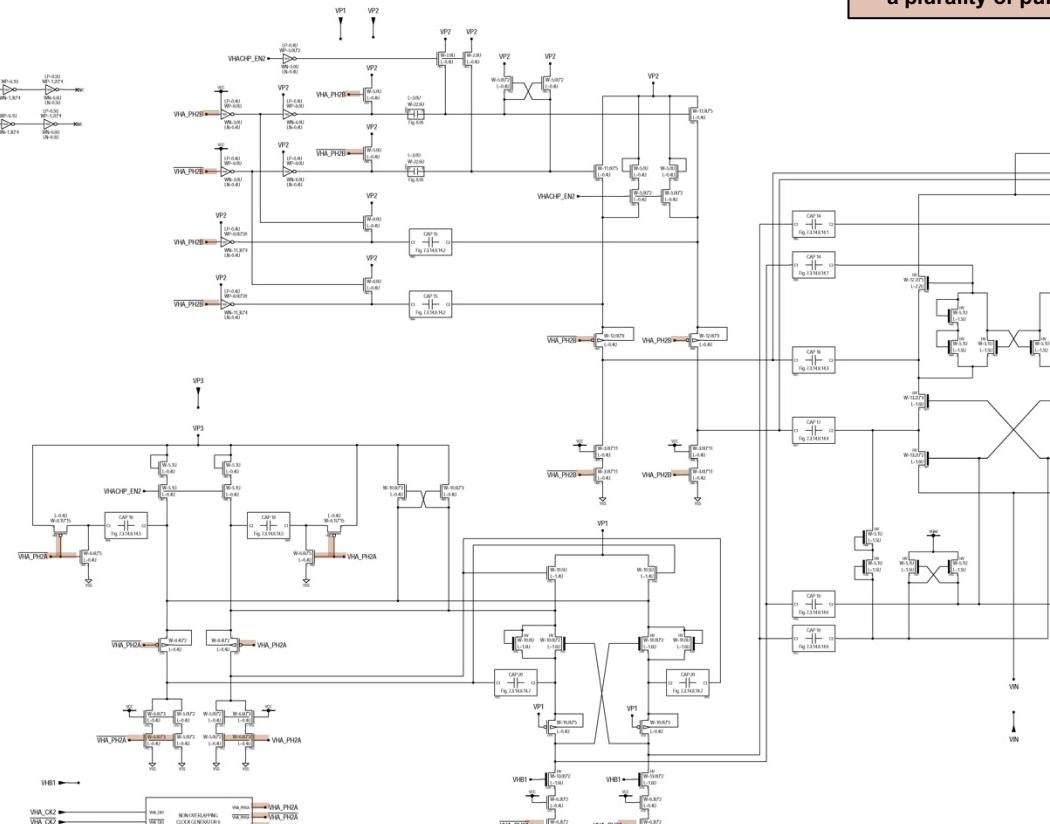
Claim 1	Accused Products
	 <p data-bbox="633 701 1848 775"> <b>Source:</b> TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4     </p>

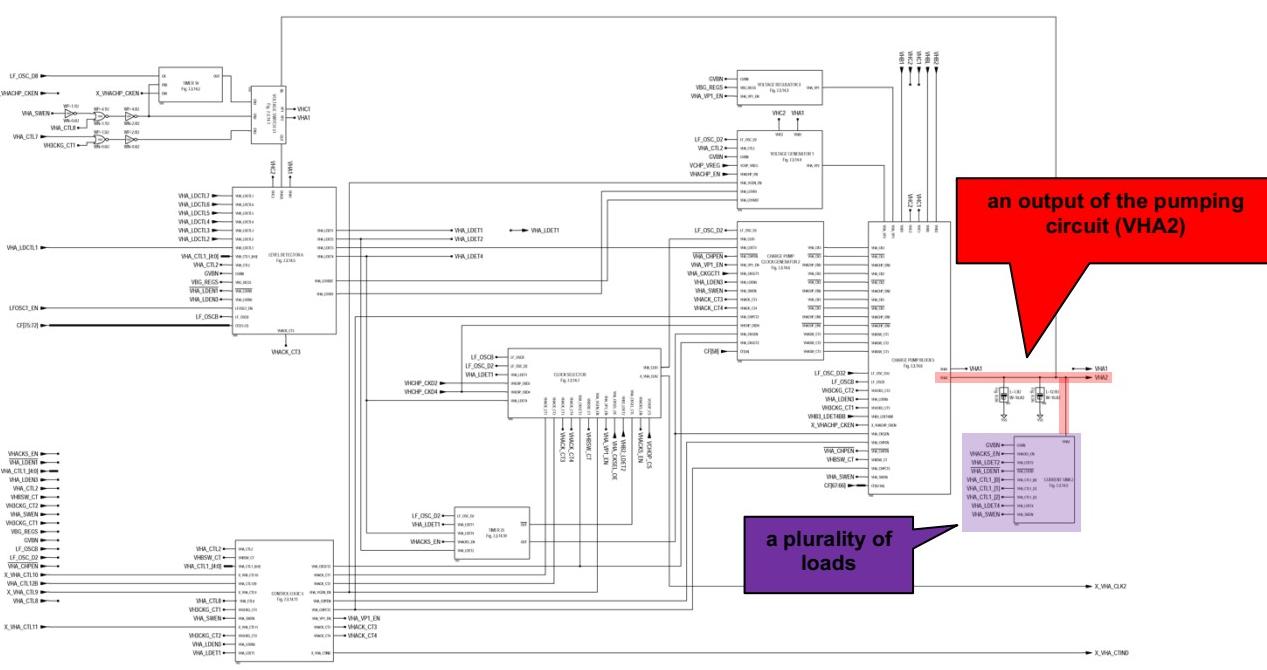
Claim 1	Accused Products
	 <p data-bbox="633 816 1837 889">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Products
	 <p data-bbox="644 995 770 1068"><b>VHA_CK2 VHA_CK2*</b></p> <p data-bbox="696 1117 887 1142">UNLabeled component specifies the sufficient bias of all input transistors and connected source/drain terminals.</p> <p data-bbox="696 1142 802 1158">Figure 7.3.14.8.14 CHARGE PUMP 13</p> <p data-bbox="1710 1117 1858 1158">Part # 109-BIA-66, F180 26G Rev. 0000 - M Date 08/01/2018 TECH INSIGHTS WWW.TECHINSIGHTS.COM Version A</p> <p data-bbox="623 1215 1826 1289">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

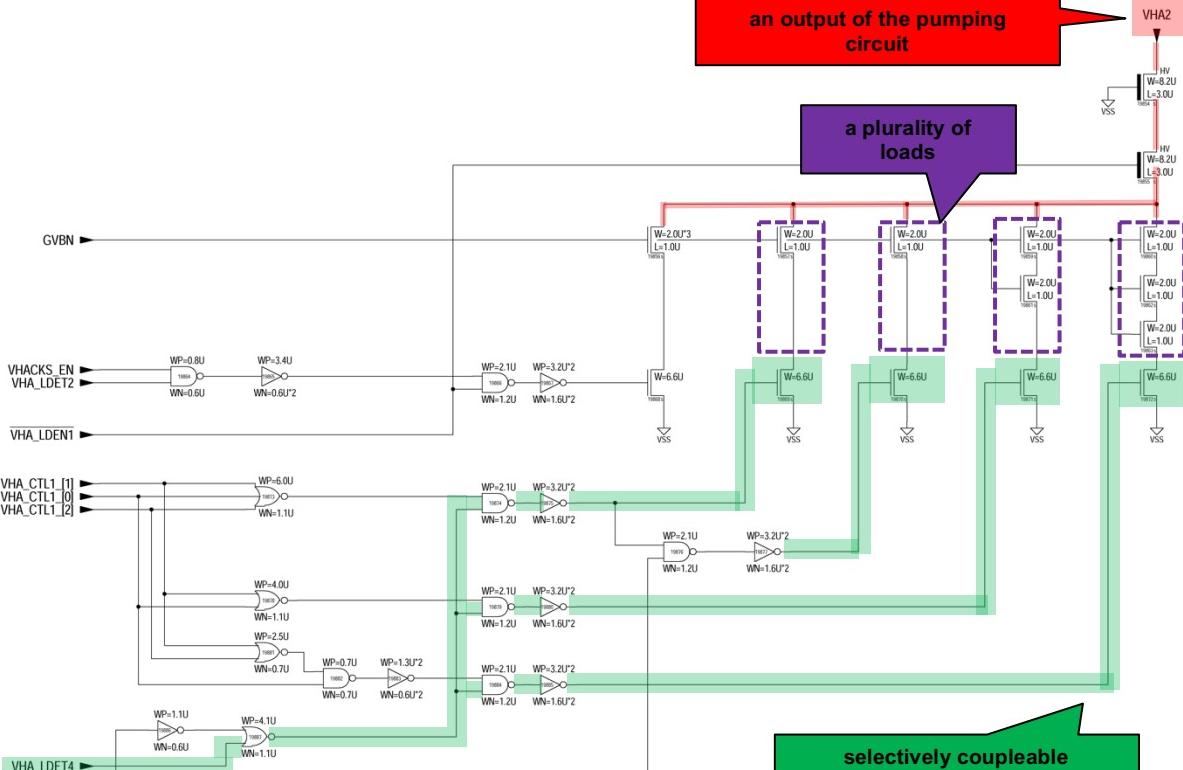
Claim 1	Accused Products
<b>VHA_CK2</b> <b>VHA_CK2*</b>	<p style="text-align: right; margin-right: 100px;"> <b>VHA_PH2A</b>  <b>VHA_PH2A*</b>  <b>VHA_PH2B</b>  <b>VHA_PH2B*</b> </p> <p style="text-align: right; margin-right: 100px;"> <i>and generate a selected one of a plurality of pump voltages</i> </p>

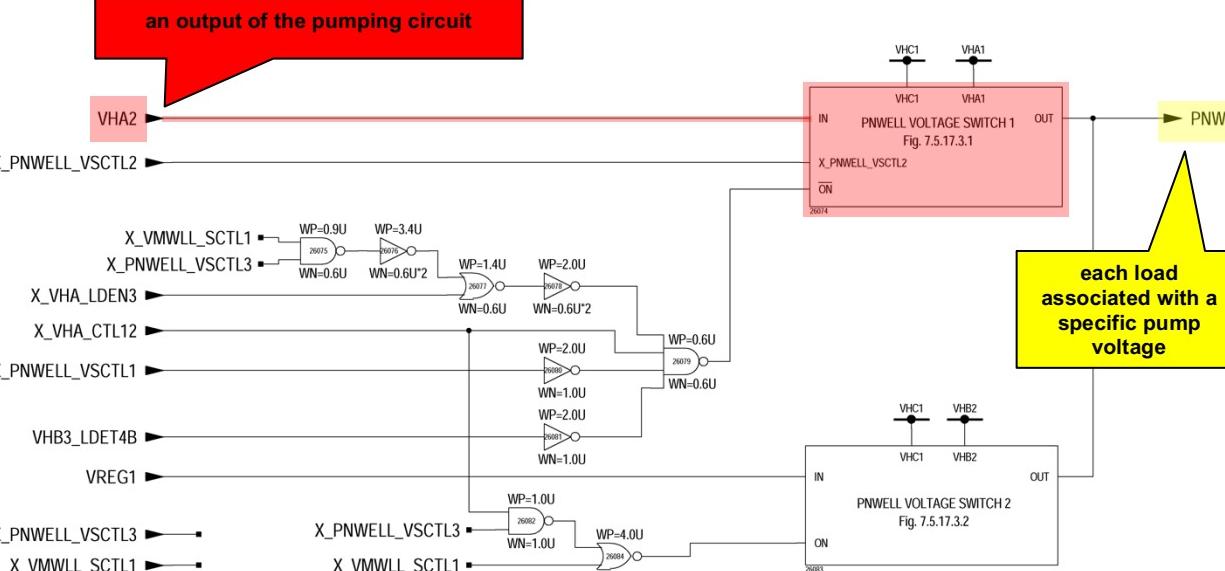
Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

Claim 1	Accused Products
<p>1[b] a plurality of loads selectively coupleable to an output of the pumping circuit,</p>	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

Claim 1	Accused Products
<p>each load associated with a specific pump voltage; and</p>	<p>For example, in the Dell/EMC XPS 15 2-in-1 9575, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p><i>See, e.g.:</i></p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

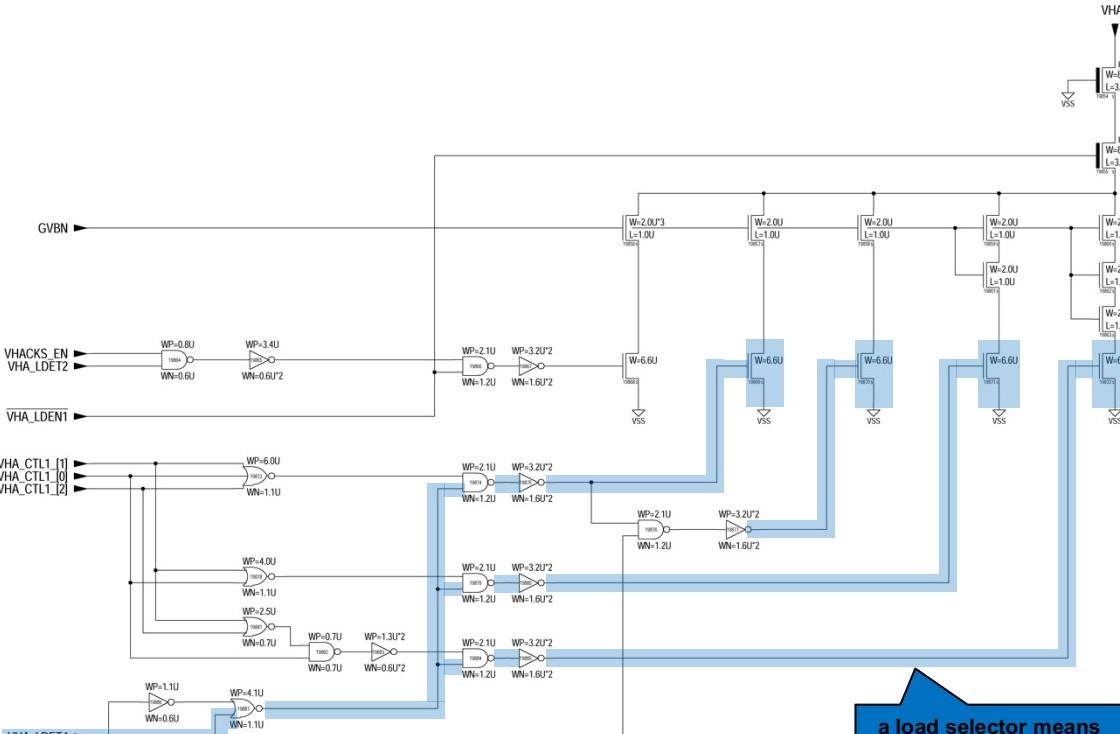


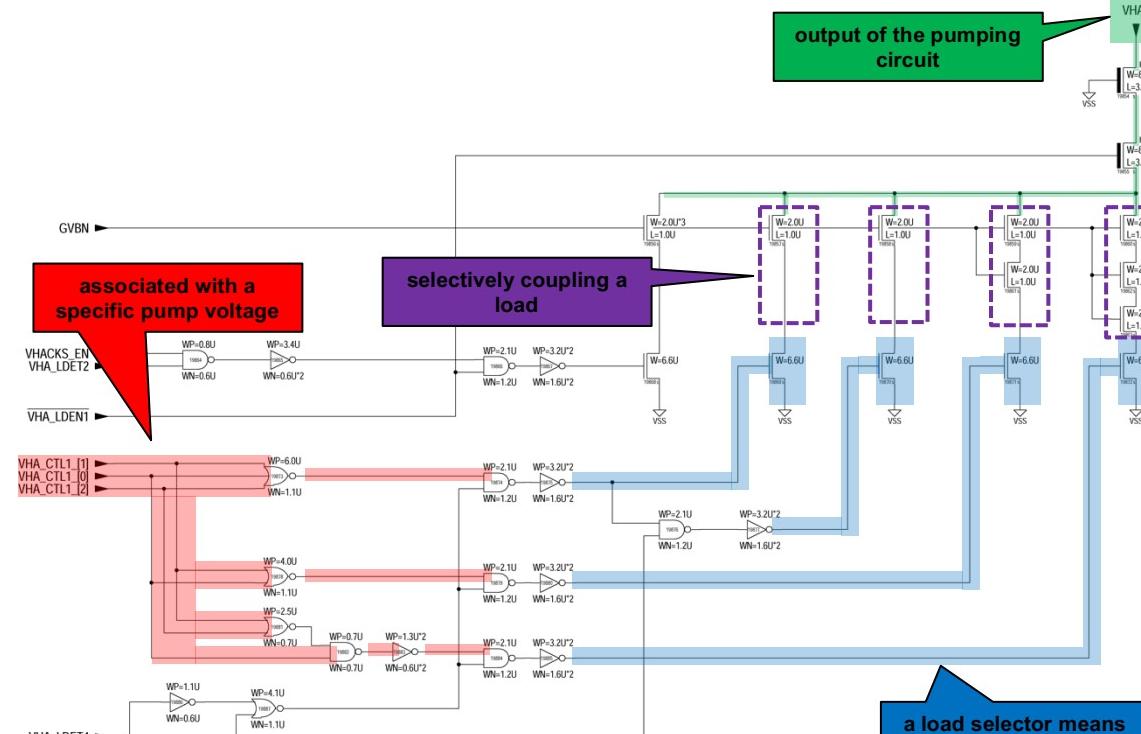
Claim 1	Accused Products
	 <p>The diagram illustrates a pumping circuit architecture. On the left, input signals include GVBN, VHACKS_EN, VHA_LDET2, VHA_LDENT1, VHA_CTL1[1], VHA_CTL1[0], VHA_CTL1[2], VHA_LDET4, and VHA_SWEN. These signals are processed through various logic gates (e.g., AND, OR, NOT) and switches (e.g., PMOS, NMOS) to control a series of current sinks. The circuit features a central current sink stage consisting of four parallel branches, each containing a PMOS switch (W=2.1U, L=1.0U) and an NMOS switch (W=3.2U, L=1.6U). The outputs of these switches connect to a common rail, which then splits into four parallel paths to drive four loads. Each load path includes a PMOS switch (W=6.6U, L=1.0U) and an NMOS switch (W=6.6U, L=1.0U). The outputs of these switches are connected to a VSS rail. A red callout box labeled "an output of the pumping circuit" points to the top right, where a VHA2 component is shown. A purple callout box labeled "a plurality of loads" points to the four parallel load paths. A green callout box labeled "selectively coupleable" points to the central current sink stage.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p data-bbox="654 881 1837 946">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
1[c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, in the Dell/EMC XPS 15 2-in-1 9575, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Products
	<p><b>a load selector means (part of)</b></p> <p>UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL MOS TRANSISTORS ARE CONNECTED TO VDD UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL MOS TRANSISTORS ARE CONNECTED TO VSS</p> <p>Figure 7.3.14.5 LEVEL DETECTOR 6</p> <p>Part #: TOSHIBA 64L FRN1 256G Date: 08/2018 Rev: 0000 S25 MMU: 1.000 S25 MMU: 0.000 TECHINSIGHTS WWW.TECHINSIGHTS.COM Version: A</p>

Claim 1	Accused Products
	 <p data-bbox="633 1060 1837 1142">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

**Claim 2**

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (<math>V_{cfra}</math>) is greater than or equal to a reference voltage (<math>V_{ref}</math>).</p>	<p>the variable charge pump circuit when the target output pump voltage (<math>V_{cfra}</math>) is greater than or equal to a reference voltage (<math>V_{ref}</math>).</p> <p>For example, in the Dell/EMC XPS 15 2-in-1 9575, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping.</p> <p><i>See evidence and explanation for claim element [1a], <i>supra</i>.</i></p>

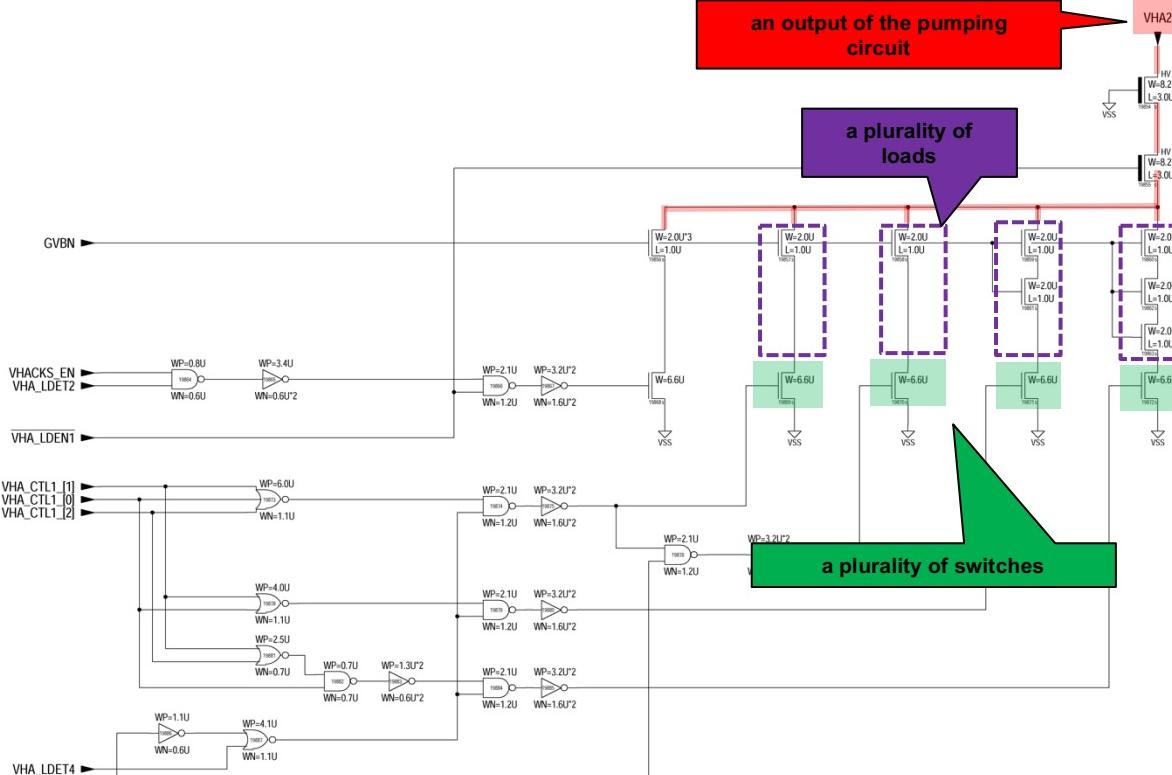
**Claim 3**

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (<math>V_{cfrb}</math>) greater than the reference voltage (<math>V_{ref}</math>) then the maximum ripple on the target output selector means adds additional loads until the <math>V_{cfrb}</math> voltage is</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (<math>V_{cfrb}</math>) greater than the reference voltage (<math>V_{ref}</math>) then the maximum ripple on the target output selector means adds additional loads until the <math>V_{cfrb}</math> voltage is less than or equal to the reference voltage (<math>V_{ref}</math>).</p> <p><i>See evidence and explanation for claim element [1a] and claim 2, <i>supra</i>.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (Vref).	

**Claim 6**

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>

Claim 6	Accused Products
	 <p data-bbox="644 1101 1848 1183">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p data-bbox="644 1199 1087 1232"><i>See also claim element [1c] supra.</i></p>

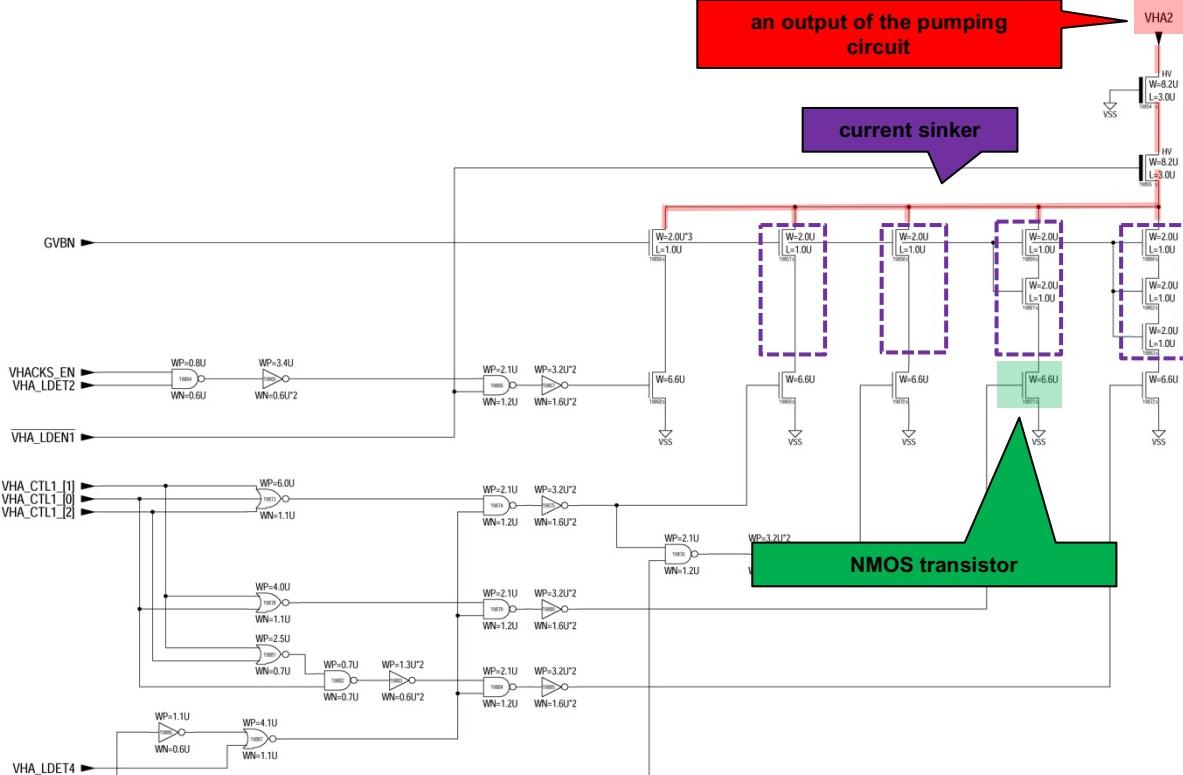
**Claim 7**

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>

Claim 7	Accused Products
	<p data-bbox="639 1111 1839 1188">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p data-bbox="639 1209 1079 1241"><i>See also claim element [1c] supra.</i></p>

**Claim 8**

Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

Claim 8	Accused Products
	 <p>The diagram illustrates a current sink circuit. It starts with an input <b>VHBNS_EN</b> which passes through a resistor (W=0.8U, L=0.6U) and an inverter (WP=3.4U, WN=0.6U). The output of this stage goes to a second inverter (WP=2.1U, WN=1.6U) followed by a resistor (W=6.6U). This signal then branches into four parallel paths, each consisting of a resistor (W=2.0U, L=1.0U) and an inverter (WP=3.2U, WN=1.6U). The outputs of these four stages are connected to the gate of a large green-shaded <b>NMOS transistor</b>. The drain of this NMOS transistor is connected to an output node <b>VHA2</b>, which is also connected to ground (VSS) via a resistor (W=8.2U, L=3.0U). The source of the NMOS transistor is connected to ground (VSS) via a resistor (W=8.2U, L=3.0U). The source of the NMOS transistor is also connected to the output node <b>VHA2</b>.</p> <p><b>Source:</b> TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p><i>See also claim element [1c] supra.</i></p>

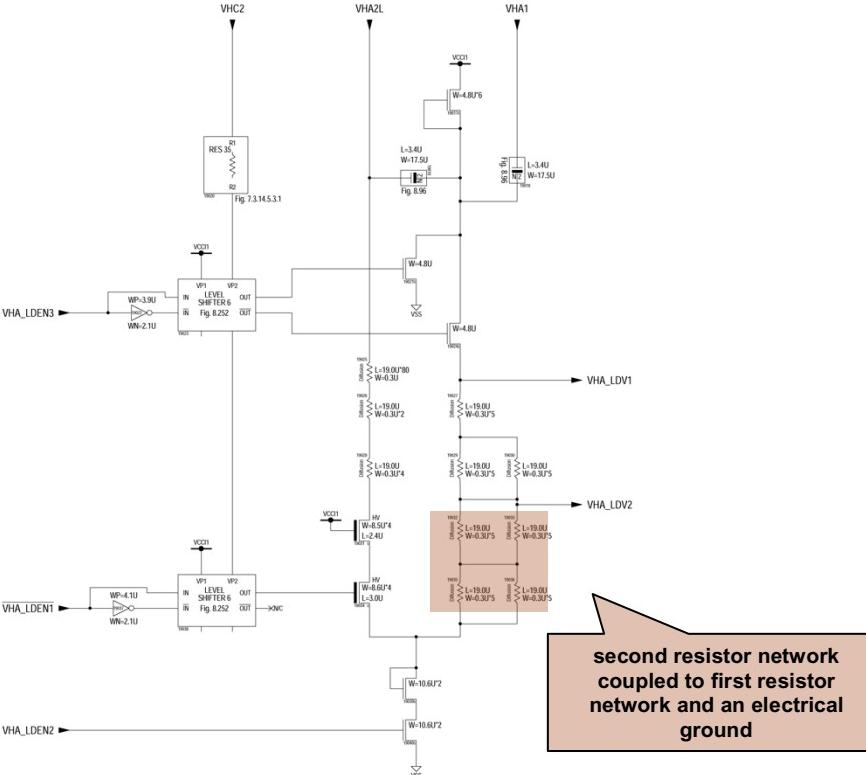
**Claim 11**

Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	<p>Each Accused Product includes the charge pump circuit of claim 2.</p> <p><i>See supra</i> claim 2.</p>
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	<p>Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref).</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator.</p>

Claim 11	Accused Products
	<p>The diagram illustrates the internal circuitry of the Sandisk/Toshiba 05138_064G 3D NAND Flash. It shows two parallel paths for voltage division. The top path starts with a resistor <b>RES35</b> (W=1.0U, L=7.3U) connected to <b>VHC2</b>. The bottom path starts with a resistor <b>RES36</b> (W=1.0U, L=7.3U) connected to <b>VHA2L</b>. Both paths feed into a <b>LEVEL SHIFTER 6</b> (VLS1 and VLS2). The outputs of these shifters are connected to a <b>COMPARATOR</b> (<b>VCA1</b>, <b>VCA2</b>, <b>VCA3</b>). The outputs of the comparators are connected to <b>AMPLIFIERS</b> (<b>VAF1</b> through <b>VAF4</b>). A red box highlights the <b>first resistor network coupled to output pump and first comparator</b>.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	<p style="text-align: center;"><b>first comparator</b></p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being coupled to an electrical ground.</p>

Claim 11	Accused Products
<p>second resistor network being coupled to an electrical ground; and</p>	 <p style="border: 1px solid black; padding: 5px; width: fit-content;">second resistor network coupled to first resistor network and an electrical ground</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
<p>[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p>

Claim 11	Accused Products
	<p>The diagram illustrates a Level Detector 6 circuit. It features four identical amplifiers (AMPLIFIER 12) arranged in a feedback loop. Each amplifier is configured with a voltage divider (VHALD_VP) and a feedback resistor (RFB). The input signal VHALD_LDET is split and fed into each amplifier. A reference voltage source (VHALD_VP) is connected to the non-inverting inputs of the amplifiers. The outputs of the amplifiers are connected to a logic gate (LEVEL SHIFTER 6) which generates the output VHALD_LDET. The circuit also includes a VHALD_LDET signal path and various control signals like GVBN, VHALD_LDET, VHALD_VP, and VHALD_LDET.</p>